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Addition and subtraction of low power logarithmic number system

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Abstract - In this article, we introduce the algorithm for the addition and subtraction of low power logarithmic number system. In this method's precision is highly dependent on the radius specified at the outset. It's likely that no part of the vector will be found during the search if the initial radius is chosen too small. It will search for points that may or may not be there if the radius is large. In our design, we used the difficult-to-understand IP core Divider and IP core Square Root.

Key Words: Addition and Subtraction, Logarithmic Number System, Low Power

1. INTRODUCTION

U. Fincke and0M. Pohst published Improved Methods for Calculating Vectors of0Short Length in a0Lattice, Including a Complexity0Analysis in [1]. Traditional approaches for calculating small-length vectors in a0lattice employ a reduction operation followed0by an enumeration of all vectors of Z "' in the suitable field It is sufficient to look into those x e Z's, though "which are contained in a0suitable ellipsoid with a volume less than the box. Oussama Damen, Ammar Chkeif, and Jean-Claude Belfiore suggested a Lattice Code Decoder for Space-Time Codes in [2]. The algebraic space–time (ST) coding and the lattice sphere packing representation of a multi-antenna system are discussed in this letter. The sphere decoding (SD) technique is used to decode the resulting lattice code. For the uncoded system, SD provides a significant improvement over the well-known V-LAST detection approach, with just a minor increase in complexity. M. Stojnic, H. Vikalo, and B. Hassibi discussed future work on speeding up the sphere decoder in[3]. In the worst-case scenario, maximum-likelihood decoding is reduced to solving an integer least-squares problem, which is NP-hard.

Emanule Viterbo and Joseph Bourto propose a Universal Lattice Code Decoder for Fading Channels in their paper[4]. When utilised over an independent fading channel with perfect channel state information at the receiver, we propose a maximum-likelihood decoding solution for any lattice code. Ecole nat proposed a Good lattice0constellations for both Rayleigh fading and Gaussian channels in [5]. Recent work on lattices0adapted to the Rayleigh0fading channel has demonstrated0how to construct signal0constellations with great spectral0efficiency. In [6], Wllon and Jon presented a method for estimating MIMO wireless multipath ray parameters based on channel transfer matrix observations. P. Blösch, P. Friedli, and A. Burg proposed a Matrix Decomposition Architecture for MIMO in [7]. In multiple-input multiple-output (MIMO) communication systems, the SVD and QRD are employed for0beamforming and0channel-matrix preprocessing for MIMO detection, respectively. Albert M. Chan Inkyu Lee presented0A New Reduced-Complexity Sphere Decoder in[8]. It's been shown that spherical decoding for multiple antenna systems can attain near-ML performance while being relatively simple.m[9] is a collaboration between T. Kailath_, H. Vikaloz, and B. Hassibiz on MIMO Receive Algorithms. In Shariat-Yazdi1 and Tad Kwasniewski presented Low Complexity Sphere Decoding Algorithms in [10]. In their paper [11], Boyu Li and Ender Ayanoglu proposed a Reduced Complexity model. In his paper [12], Haris Vikalo Bahak Hassibi proposed an On the Sphere Decoding Algorithm. II. Applications of Generalizations, Second-Order Statistics, and Communications. Luis G. Barbero and John S. Thompson created a fixed-complexity mimo detector based on the complex sphere decoder in 2013. For uncoded multiple input-multiple output (MIMO) systems, this work provides a new detection algorithm based on the complicated version of the sphere decoder (SD). Fei Zhao and Sanzheng Qiao published Radius Selection Algorithms for Sphere Decoding in [14]. The integer least squares problem is used in a variety of applications, including communications, cryptography, and GPS. Area and Delay Trade-offs in FPGA Circuit and Architecture Design[15] was presented0by Ian Kuon and0Jonathee Rose. Leakage0current is also important for power0regulation in low-power0VLSI devices. As a fraction of overall integrated circuit power dissipation, leakage current is becoming increasingly important. Several low-power circuit and system ideas, approaches, and power management techniques are discussed in this work. The challenges of building low-power, high-performance circuits in the future are also discussed.

2. DESIGN CIRCUIT

The entire thesis is broken into three modules for coding:

a) Design of Newton Algorithm
b) Design of Q-Cholesky Algorithm
c) Design of Sphere Decoding Algorithm

a) Newton Algorithm

We utilise a Finite State Machine to code our architecture because this approach demands matrix multiplication at each iteration. In order to determine Norm 1 and Norm, we employ two FSMs in our code: one for matrix multiplication and the other for comparing multiple rows and column values.

First iteration coding:

- The channel matrix is used as the Newton algorithm's input matrix, and the norm of the matrix is obtained during the first iteration.
- As a result, the code for Norm 1 and Norm Infinity calculations is created. This calculation requires multiplying the matrix's row and column components, then comparing the resultant elements to see which has the highest value.
- These calculated norms are divided by one after being multiplied by one. The transpose matrix of the channel Matrix will be multiplied by the division result.
- The outcome of the above point will be subtracted from the Identity Matrix. Instead of establishing the

Identity Matrix, we simply subtract the diagonal elements from 2 and the rest ones from 0. This lowers the Hardware of the Design.

- It is then used to iterate from 1 to 7 using the Finite State Machine. The first iteration's output is used as the input matrix for the next iteration.
- In the seventh iteration, we calculate the Residue matrix.
- To observe the convergent behaviour of the Newton algorithm.
- The Matrix obtained after the seventh iteration is known as the pseudo inverse Matrix.
- The I Matrix is created by multiplying the Received Vector Matrix by the pseudo inverse Matrix. This I matrix will be used in the SD approach.

b) Q-Cholesky Algorithm

The matrix is partitioned into the Upper triangular matrix using this way. To obtain the gramme matrix, we employ two FSM: one for matrix multiplication and the other for matrix multiplication. The upper triangular Matrix is created in the second stage.

- The Gram Matrix is formed by multiplying the Channel Matrix by its transposition. The "Q-Chol" Algorithm uses this Gram matrix as an input.
- Using the gauss-Jordan(discussed in chapter4) row transformation methods, the Gram matrix decomposes into an Upper Triangular matrix.
- On the basis of the Gauss-Jordan method's results, several multiplication and division operations are performed.
- A q-matrix matrix will be used in the SD method.

c) Sphere Decoding Algorithm

This section will just cover the step that was utilised to develop the algorithm.

- To create the complete approach, we use a single FSM input given to the algorithm, which is a Q-matrix and an I matrix.

The algorithm proceeds according to the states defined in the technique, resulting in the Minimum Euclidian distance vector and the Transmitter's Input Matrix.

For example, a crossbar switch requires much more routing than a systolic array with the same gate count. Since unused routing tracks increase the cost (and decrease the performance) of the part without providing any benefit, FPGA manufacturers try to provide just enough tracks so that most designs that will fit in terms of Lookup tables (LUTs) and I/Os can be routed. In general, a logic block (CLB or LAB) consists of a few logical cells (called ALM, LE, Slice etc.). A typical cell consists of a 4-input LUT, a Full adder (FA) and a D-type flip-flop, as shown below as shown in Fig.1. The LUTs are in this figure split into two 3-input LUTs. In normal mode those are combined into a 4-input LUT through the left mux. In arithmetic mode, their outputs are fed to the FA.

3. SIMULATION RESULT

We are developing a 2x2 MIMO system with a 4x4 channel matrix. The QAM Modulation technique is crucial to our entire effort. The shortest radius is efficiently obtained, but there are a few challenges along the way, such as choosing a channel matrix that is random in nature, non-singular, and capable of generating the upper triangular matrix when multiplied with its transpose. The sphere's starting radius is the second problem to solve. This synthesis result was created using the IP Core Divider and Square Root. We devised two designs, one for stimulation and the other for synthesis, because the findings produced by the core are difficult to comprehend.

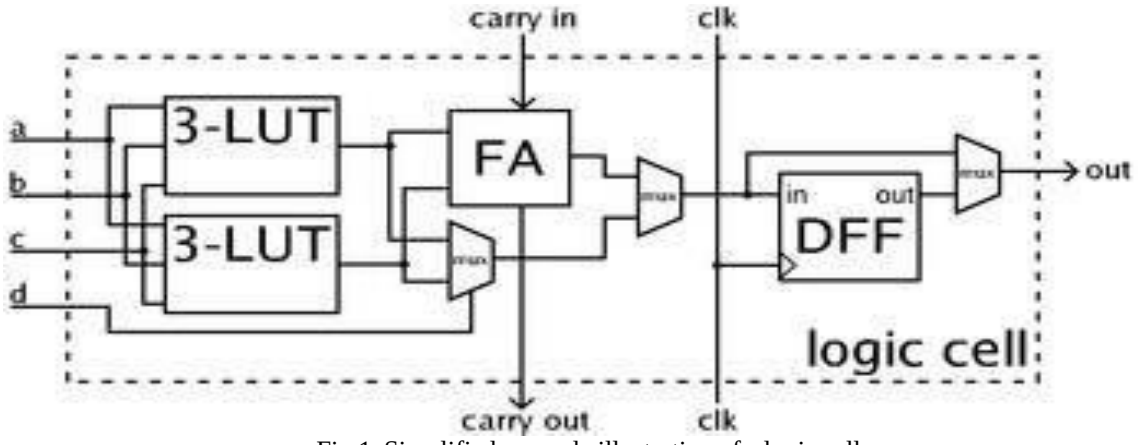

Fig.1. Simplified example illustration of a logic cell

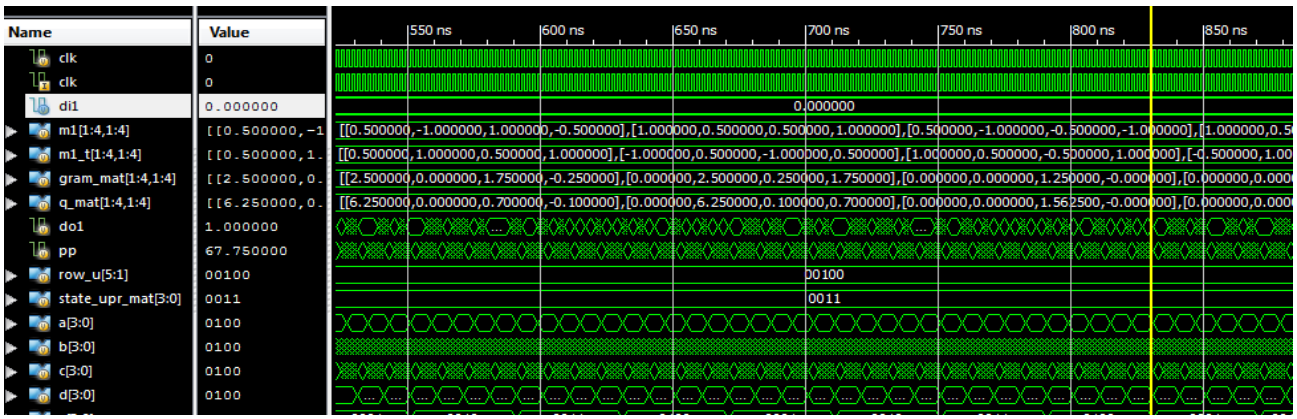

Fig.2 Q-Chol

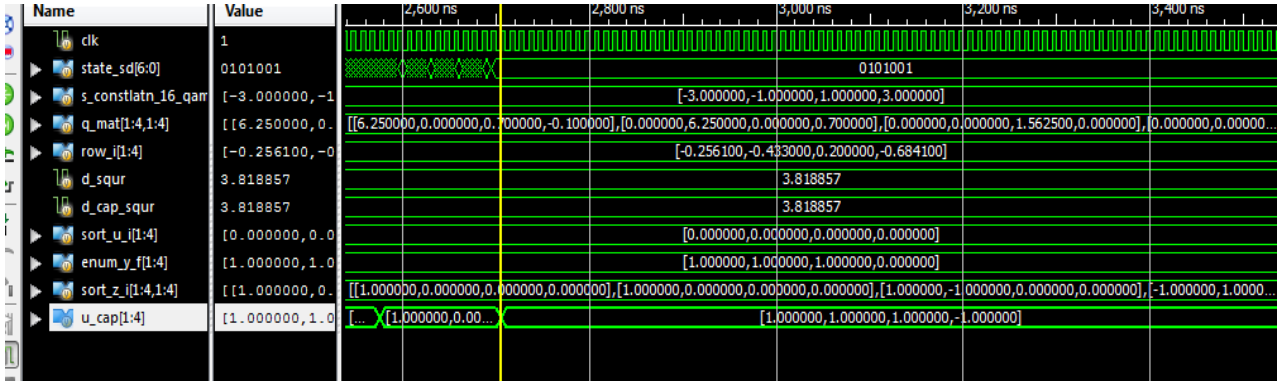

Fig.3 SD algorithm

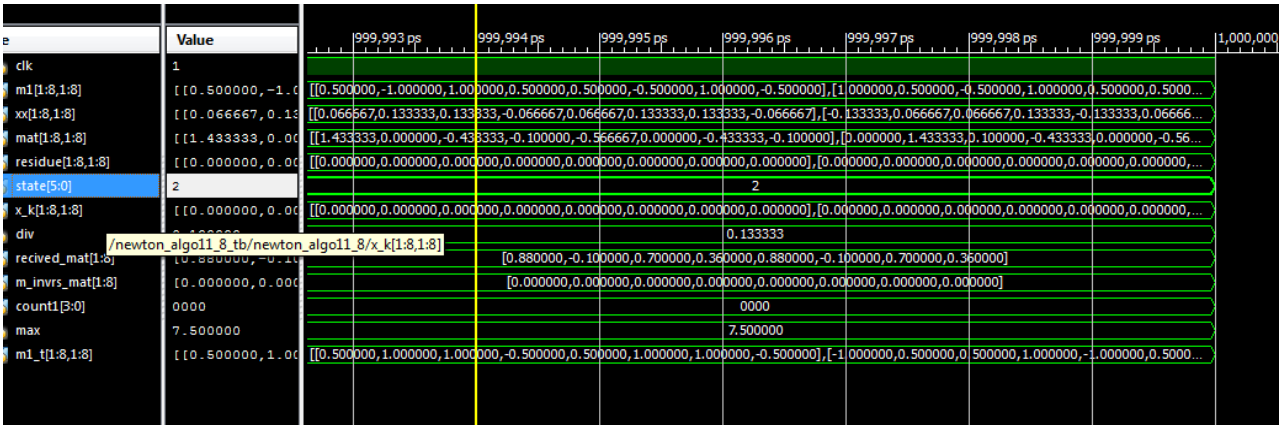

Fig.4. Newton algorithm4x4 MIMO

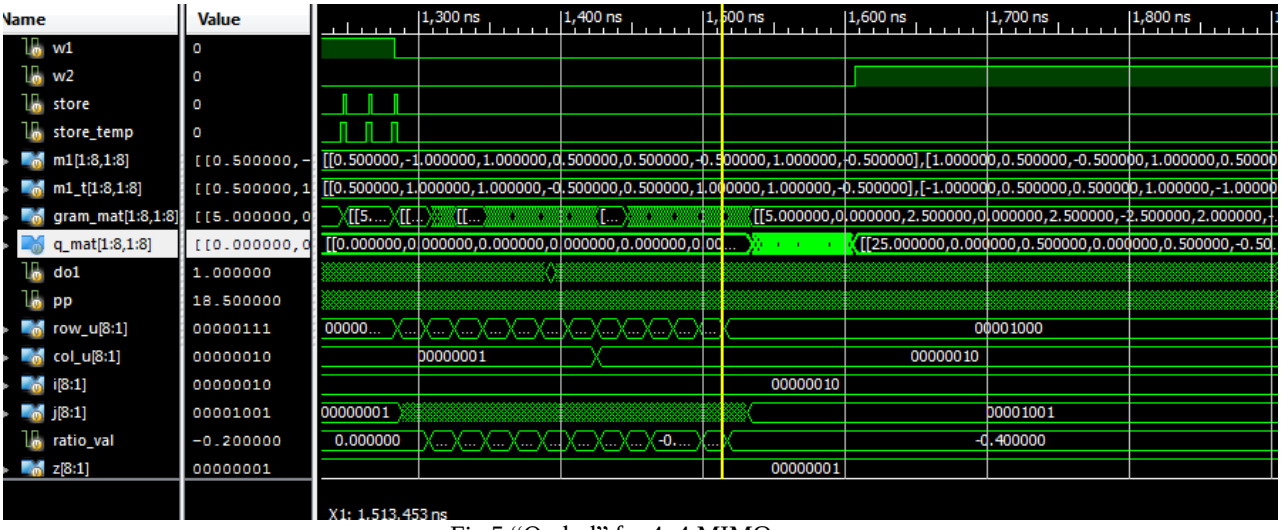

Fig 5 “Q-chol” for 4x4 MIMO

3. CONCLUSIONS

The overall conclusion of the study is that while picking the shortest distance vector, the SD algorithm has a number of flaws. The method's precision is highly dependent on the radius specified at the outset. It's likely that no part of the vector will be found during the search if the initial radius is chosen too small. It will search for points that may or may not be there if the radius is large. In our design, we used the difficult-to-understand IP core Divider and IP core Square Root. As a result, the design can be further enhanced.

REFERENCES

1. V. Mahalingam and N. Ranganathan, "Improving Accuracy in Mitchell's Logarithmic Multiplication using Operand Decomposition,"IEEE Trans. Computers, vol. 55, no. 12, pp. 1523-1535, Dec.2006.
2. K. Johansson, O. Gustafsson, and L. Wanhammar, "Implementation of Elementary Functions for Logarithmic Number Systems," IET Computers and Digital Techniques, vol. 2, no. 4, pp. 295-304,http://link.aip.org/link/?CDT/2/295/1, 2008.
3. M.G. Arnold, T.A. Bailey, J.R. Cowles, and M.D. Winkel,"Arithmetic Co-Transformations in the Real and Complex Logarithmic Number Systems," IEEE Trans. Computers, vol. 47,no. 7, pp. 777-786, July 1998.
4. V.S. Dimitrov, G.A. Jullien, and W.C. Miller, "Theory and Applications of the Double-Base Number System," IEEE Trans.Computers, vol. 48, no. 10, pp. 1098-1106, Oct. 1999.
5. R. Muscedere, V. Dimitrov, G. Jullien, and W. Miller, "Efficient Techniques for Binary-to-Multidigit Multidimensional Logarithmic Number System Conversion using Range-Addressable Look-Up Tables," IEEE Trans. Computers, vol. 54, no. 3, pp. 257-271,Mar.2005
6. R.C. Ismail and J.N. Coleman, "ROM-less LNS," Proc. IEEE Symp.Computer Arithmetic,pp. 43-51, 2011.
7. H. Fu, O. Mencer, and W. Luk, "FPGA Designs with Optimized Logarithmic Arithmetic,"IEEE Trans. Computers, vol. 59, no. 7,pp. 1000-1006, July 2010.
8. M. Arnold and S. Collange, "A Real/Complex Logarithmic Number System ALU," IEEETrans. Computers, vol. 60, no. 2, pp. 202-213, Feb. 2011.
9. F.J. Taylor, R. Gill, J. Joseph, and J. Radke, "A 20 bit Logarithmic Number System processor," IEEE Transactions on Computers, vol. 37, no. 5, pp. 190–199, Feb. 1988.
10. Costas Efstathiou, Haridimos T. Vergos, and Dimitris Nikolos, "Modulo 2 n +1adder design using select-prefix blocks," IEEE Transactions on Computers, vol. 52, no. 11, Nov.2003.
10. S. Paul, N. Jayakumar, and S. Khatri, "A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm Computations,"IEEE Trans. Very Large Scale Integration Systems, vol. 17,no. 2, pp. 269-277, Feb. 2009.
11. J. Kurokawa, T. Payne, and S. Lee, "Error Analysis of Recursive Digital Filters Implemented with Logarithmic Number Systems,"IEEE Trans. Acoustics, Speech, and Signal Processing, vol. 28, no. 6,pp. 706-715, Dec. 1980.
12. F. Taylor, R. Gill, J. Joseph, and J. Radke, "A 20 bit Logarithmic Number System Processor," IEEE Trans. Computers, vol. 37, no. 5,pp. 190-199, Feb. 1988.
13. M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi, Low Power Methodology Manual: For System-on-Chip Design. Springer Publishing Company, Inc., 2007.
14. C.-H. Chang, J. Chen, and A. Vinod, "Information Theoretic Approach to Complexity Reduction of FIR Filter Design," IEEE Trans. Circuits and Systems - Part I, vol. 55, no. 8, pp. 2310-2321,Sept. 2008.
15. M. Aktan, A. Yurdakul, and G. Dundar, "An Algorithm for the Design of Low-Power Hardware-Efficient FIR Filters," IEEE Trans. Circuits and Systems - Part I, vol. 55, no. 6, pp. 1536-1545, July 2008.